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This book presents a novel approach to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-

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to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion.

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Modeling...

The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-

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delta modulation
and time-to-digital
conversion.

Readers will gain a
deep
understanding of
ADPLLs and the
central role played
by noise-shaping.

Processing

This book presents
a novel approach

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to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping.

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Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion.

Readers will gain a deep understanding of ADPLLs and the central role played

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by noise-shaping. A range of ADPLL and TDC architectures are presented in unified manner.

Analytical and simulation tools are discussed in detail.

Matlab code is included that can be reused to

design, simulate and analyze the ADPLL

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architectures that
are presented in
the book.

Loops Modeling

This book presents
a novel approach
to the analysis and
design of all-digital
phase-locked loops
(ADPLLs).

technology widely
used in wireless
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conversion.

Readers will gain a deep

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Analytical and

simulation tools are

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Matlab code is included that can be reused to design, simulate and analyze the ADPLL architectures that are presented in the book.

Processing

Time-to-digital converter (TDC) circuits are a key component for

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achieving high-performance digital phase-locked loops (PLLs) which offer lower area and greater flexibility than their analog PLL counterparts.

This chapter focuses on a recently developed TDC architecture known as the gated ring oscillator

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(GRO) which offers first-order shaping of its quantization noise and delay stage mismatch. To provide context for the GRO discussion, background on general TDC implementation techniques is described along with key

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performance issues related to digital frequency synthesizers. The GRO concept is then presented, followed by implementation details and measured results. Finally, recent variations on the GRO concept are described such as

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a MASH TDC structure which achieves higher-order noise shaping and a switched ring oscillator (SRO) TDC which improves robustness to dead zones encountered by the GRO TDC.

In this dissertation,
time-based signal

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processing techniques and their applications in phase-locked loops, modeling and simulation, and noise-shaping data converters are examined. These techniques demonstrate the ability to shift the burden of high performance analog circuits from the

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compressed
voltage-domain to
the augmented
time-domain. First,
the potential of
high order noise-
shaping and phase-
domain feedback in
time-to-digital
converters (TDCs)
is explored. A
prototype phase
reference, second-
order continuous-

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time delta-sigma
TDC for sensor
applications was
fabricated in 90nm
CMOS and achieves
64 dB dynamic
range in 1MHz
signal bandwidth.
Second, an ultra-
high performance
oscillator-based
delta-sigma
modulator
architecture is

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investigated. The proposed circuit is a third-order continuous-time PLL-Based Delta-Sigma Modulator with simulated 77 dB SNDR in 40MHz signal bandwidth with OSR of 16, and is fabricated in 65nm CMOS.

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Giving a basic overview of the technologies supporting cognitive radio this introductory-level text follows a logical approach, starting with the physical layer and concluding with applications and general issues. It

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medium access control and network layer design are examined before the book concludes by covering the topics of trusted cognitive radio networks and spectrum management.

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Simulation Ysis

This book describes
several Digital
Delta-Sigma

Modulator (DDSM)
architectures,

including multi
stage noise

shaping (MASH),
error feedback

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modulator (EFM)

and single
quantizer

(SQ)-DDSM

modulators, with a
focus on predicting
and maximizing
their cycle lengths.

The authors aim to
demystify an
important aspect of
these particular
DDSM structures,
namely the

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existence of spurs resulting from the inherent periodicity of DDSMs with constant inputs. Simulink and MATLAB models and code are presented in Chapters 2–5 to enable the reader to reproduce the results in this work and to explore

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further. These examples will also be helpful for first-time designers of DDSMs.

In less than one decade after their introduction into radio-frequency applications, digital fractional-N phase-locked loops (PLLs) have become a

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relevant topic in
microelectronic
research and a
practical solution
for products. In
addition to the well-
known advantages,
such as their silicon
area occupation
scaling as
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and their easier
portability to new
nodes, digital PLLs

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enable easy and low-cost implementation of calibration techniques, which substantially reduce spurious tones and remove other major analog impairments. In wideband PLLs, the ultimate level of spur performance is often bounded

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All the time resolution and the linearity of the time-to-digital converter within the digital PLL. Methods for mitigating its nonlinearity such as those based on element randomization and large-scale dithering are discussed. The use

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of fractional-N dividers based on digital-to-time converters, as a means to relax the design of the time-to-digital converter, is also reviewed.

This concept is extended to the limit case of a single-bit time-to-digital converter, which provides

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best PLL
noise-power trade-
off with good spur
performance.

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The book offers
unique insight into
the modern world
of wireless
communication
that included 5G
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In three parts, this book contributes to the advancement of engineering

education and that serves as a general reference on digital signal processing.

Part I presents the basics of analog and digital signals and systems in the time and frequency domain. It covers

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the core topics:
convolution,
transforms, filters,
and random signal
analysis. It also
treats important
applications
including signal
detection in noise,
radar range
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systems, channel estimation, banking and financial applications, and audio effects production. Part II considers selected signal processing systems and techniques. Core topics covered are the Hilbert transformer, binary signal

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transmission,
phase-locked
loops, sigma-delta
modulation, noise
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